WHAT IS CLAIMED IS:

1. A telecommunications chassis, comprising:

a shielding chamber having a first and second horizontal surface and a first and second vertical surface, the first and second vertical surfaces being disposed between the first and second horizontal surfaces, wherein the first and second horizontal surfaces and the first and second vertical surfaces are made of metal and are conductively connected;

a vertical backplane having connectors for interfacing with repeater modules, the vertical backplane being disposed between the first and second horizontal surfaces and the first and second vertical surfaces, the vertical backplane establishing contact with the first and second horizontal surfaces and the first and second vertical surfaces, the vertical backplane having a ground conductor electrically connected to the connectors;

an outer housing encompassing the shielding chamber and the vertical backplane and having an open side for receiving telecommunications modules, and the outer housing having a first cover surface that is substantially parallel to but within a different spatial plane from the first horizontal surface and having a second cover surface that is substantially parallel to but within a different spatial plane from the vertical backplane, wherein spacing between the first cover surface and the first horizontal surface and spacing between the second cover surface and the vertical backplane form an airspace; and

a chassis ground conductor electrically connected to the shielding chamber and the ground conductor of the vertical backplane.

2. The telecommunications chassis of claim 1, wherein the outer housing further includes a third cover surface that is substantially parallel to but within a different spatial plane from the second horizontal surface, the third cover surface having a plurality of holes adjacent to the airspace.

3. The telecommunications chassis of claim 1, wherein the second cover surface has a plurality of holes adjacent to the airspace.

4. The telecommunications chassis of claim 1, further comprising a faceplate substantially parallel to but within a different spatial plane from the vertical

backplane, the faceplate being disposed within the open side of the outer housing, the faceplate for contacting telecommunications modules installed in the chassis, the faceplate having an aperture for receiving telecommunications modules.

5. The telecommunications chassis of claim 1, further comprising a housing door hinged to the outer housing at the open side.

6. The telecommunications chassis of claim 1, further comprising a handle rotatably mounted to the outer housing.

7. The telecommunications chassis of claim 1, wherein the first and second horizontal surfaces have longitudinal slots for guiding and receiving telecommunications modules.

8. The telecommunications chassis of claim 4, wherein the first and second horizontal surfaces have longitudinal slots for guiding and receiving telecommunications modules, and the faceplate has notches that align with the slots.

9. The telecommunications chassis of claim 1, wherein the first and second horizontal surfaces have a plurality of holes.

10. The telecommunications chassis of claim 1, further comprising a power supply mounted to the second cover surface and disposed within the airspace.

11. The telecommunications chassis of claim 1, wherein the outer housing is made of metal and the chassis ground conductor is conductively connected to the outer housing.

12. The telecommunications chassis of claim 1, further comprising a plurality of repeater modules disposed within the shielding chamber and interfaced with the vertical backplane, the repeater modules having circuitry enclosed within a shell, the shell having a first shell surface for engaging the first horizontal surface and a second shell surface for engaging the second horizontal surface.

13. The telecommunications chassis of claim 12, wherein the circuitry receives a monitor signal, amplifies the monitor signal to generate an amplified monitor signal, recovers data and clock information from the amplified monitor signal, and produces an output signal repeating the recovered data and clock information, and wherein the monitor signal and the output signal have data rates greater than about 52 megabits per second.

14. The telecommunications chassis of claim 1, wherein the top and bottom horizontal surfaces have a zinc chromate plating.

15. A telecommunications circuit module, comprising:

a printed circuit board including circuitry;

a metal backplate substantially parallel to but within a different spatial plane from the printed circuit board;

a metal shell having a frontplate, a top surface perpendicular to and extending from the frontplate, a bottom surface substantially parallel to the top surface and extending from a side of the frontplate away from the top surface, and a back surface perpendicular to the front plate and the top and bottom surfaces, wherein the top surface, bottom surface, and back surface each has a folded edge that abuts the metal backplate to establish metal to metal contact; and

a metal jack holder extending perpendicularly from the printed circuit board and abutting the front plate, top surface, and bottom surface to establish metal to metal contact along a side away from the back surface, and wherein at least a portion of the circuitry is disposed between the frontplate and the backplate and between the metal jack holder and the back surface.

16. The telecommunications circuit module of claim 15, wherein the top and bottom surfaces of the metal shell have a plurality of holes.

17. The telecommunications circuit module of claim 16, wherein the metal backplate, metal shell, and metal jack holder are aluminum.

18. The telecommunications circuit module of claim 15, wherein the circuitry includes repeater circuitry receiving an input signal, recovering data and clock

information from the input signal, and creating an output signal repeating the data and clock information.

19. The telecommunications circuit module of claim 18, wherein the input signal is a monitor signal, the repeater circuitry including an amplification portion with a current feedback operational amplifier and a voltage limiting operational amplifier and including a transceiver portion.

20. The telecommunications circuit module of claim 19, wherein the monitor signal and the output signal have data rates greater than about 52 megabits per second.

21. The telecommunications circuit module of claim 15, wherein the metal backplate has mounting fins extending from the edges contacting the top and bottom surfaces of the metal shell.

22. The telecommunications circuit module of claim 15, wherein the backsurface has an aperture surrounding a connector extending from the printed circuit board.

23. The telecommunications circuit module of claim 15, further comprising a faceplate abutting the metal jack holder.

24. A repeater circuit comprising:

an amplification portion that receives a first signal with data and clock information and increases the amplitude of the first signal to generate an amplified first signal, the amplification portion including a current feedback amplifier stage and a voltage limiting amplifier stage; and

a transceiver portion that receives the amplified first signal, recovers the data and clock information from the received amplified first signal, and transmits a second signal with the data and clock information recovered from the amplified first signal.

25. The repeater circuit of claim 24, wherein the first signal is a monitor signal and wherein the amplified first signal is about 0.5 volts peak-to-peak.

26. The repeater circuit of claim 24, further comprising a first isolation transformer for passing the first signal to the amplification portion and a second isolation transformer for receiving the second signal from the transceiving portion.

27. The repeater circuit of claim 24, where the first signal and the second signal have data rates greater than about 52 megabits per second.

28. The repeater circuit of claim 24, wherein the first signal is amplified by the current feedback amplifier stage prior to being amplified by the voltage limiting amplifier stage.

29. The repeater circuit of claim 24, further comprising:

a reference clock providing a reference clock signal to the transceiver; and

a programmable logic device in communication with the transceiver and external visual indicators.

30. The repeater circuit of claim 24, further comprising:

a first isolation transformer;

a printed circuit board housing the first isolation transformer, current feedback amplifier stage, voltage limiting amplifier stage, and the transceiver portion;

a first linear signal trace connecting the first isolation transformer to the current feedback amplifier stage; and

a second linear signal trace connecting the current feedback amplifier stage to the voltage limiting amplifier stage, wherein the first signal trace is positioned linearly with respect to the second signal trace.

31. The repeater circuit of claim 30, wherein each continuous piece of the first linear signal trace and the second linear signal trace is less than one-fourth of an inch in length.

32. The repeater circuit of claim 30, further comprising:

an input jack;

an output jack;

a second isolation transformer;

a third signal trace connecting the input jack to the first isolation transformer;

a fourth signal trace connecting the voltage limiting amplifier stage to the transceiver portion;

a fifth signal trace connecting the transceiver portion to the second isolation transformer; and

a sixth signal trace connecting the second isolation transformer to the output jack, wherein the first and second linear signal traces and the third, fourth, fifth, and sixth signal traces lie within the same spatial plane on the printed circuit board.

33. The repeater circuit of claim 30, further comprising:

an input jack;

an output jack;

a second isolation transformer;

a third signal trace connecting the input jack to the first isolation transformer;

a fourth signal trace connecting the voltage limiting amplifier stage to the transceiver portion;

a fifth signal trace connecting the transceiver portion to the second isolation transformer; and

a sixth signal trace connecting the second isolation transformer to the output jack, wherein the first and second linear signal traces and the third, fourth, fifth, and sixth signal traces have a continuous trace width.

34. The repeater circuit of claim 24, wherein the repeater circuit is for placement within a chassis having a chassis ground, the repeater circuit further comprising:

a connector having a two-dimensional array of conductive pins, wherein at least 75% of the pins are electrically connected to the chassis ground; and

a printed circuit board housing the amplification portion, transceiver portion, and the connector.

35. The repeater circuit of claim 34, wherein the printed circuit board has a plurality of layers, with the plurality of layers including a ground plane made of a continuous plane of copper, the ground plane being electrically connected to the plurality of pins electrically connected to the chassis ground.

36. The repeater circuit of claim 35, wherein the plurality of layers further includes a power layer within a center area of the printed circuit board adjacent to the ground plane and includes a plurality of dielectric layers, wherein the thickest dielectric layer is disposed between the power and ground planes.

37. The repeater circuit of claim 24, further comprising:

an oscillator; and

an oscillator signal trace connecting the oscillator to the transceiver portion, the oscillator signal trace having a length less than 0.8 inches.